Remarks

Applicants respectfully request that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicants submit that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicant believes that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

No claims have been amended. No claims have been canceled. Therefore, claims 48-76 are now presented for examination.

Claims 48-76 stand rejected under 35 U.S.C. §102 (b) as being unpatentable over Incardona et al. (EP 274045 A1). Applicants submit that the present claims are patentable over Incardona.

Incardona discloses an electronic odometer provided with a non-volatile, non-programmable memory (for example of PROM type) for the more significant digits, and a volatile memory (for example of RAM type) for the less significant digits. See Incardona at Abstract.

Claim 48 of the present application recites:

> A method comprising:
> maintaining a first value for a first counter based on a content of a volatile memory;
> maintaining a second value for a second counter based on a content of a non-volatile memory; and
> controlling updates to the first value for the first counter and to the second value for the second counter, the first and second values used to generate a monotonic count.

Applicants submit that nowhere in Incardona is there disclosed a counter having volatile and non-volatile memories to generate a monotonic count. Nevertheless, the Examiner maintains that:

> Incardona et al clearly disclose using the counters to generate a monotonic count. Incardona et al discloses

> using tow counters, volatile memory [fig. 1, volatile memory 13] and non-volatile memory [fig. 1, non-volatile memory 20] to generate a monotonic count, the electronic odometer reading that is displayed on a display unit [fig. 1, display unit 27, col. 3, lines 50-54].

See Final Office Action at page 2, paragraph 7.

Applicants disagree with the Examiners characterization of the Incardona reference. Particularly, applicants submit that an electronic odometer using a non-volatile memory for more significant digits and volatile memory for the less significant digits is not comparable to a monotonic counter. One of ordinary skill in the art will recognize that a monotonic count is generated by a monotonic counter, which is used for synchronizing software threads. For instance, a monotonic counter may used for the application of threads to multiprocessing. Moreover, applicants describe in the specification that monotonic counters are used in computer systems. See specification at page 1. Therefore, the Incardona odometer does not disclose a first value for a first counter and a second value for a second counter wherein the first and second values are used to generate a monotonic count. Accordingly, claim 1 is patentable over Incardona.

Claims 49-53 depend from claim 48 and include additional limitations. Therefore, claims 49-53 are also patentable over Incardona.

Claim 54 recites:

> A method comprising:
>
> reading a count value for a monotonic counter, the monotonic counter at least partially basing the count value on a content of a volatile memory and a non-volatile memory; and
>
> updating the count value for the monotonic counter by utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.

Thus, for the reasons described above with respect to claim 48, claim 54 is patentable over Incardona. Since claim 55 depends from claim 54 and includes additional limitations, claim 55 is also patentable over Incardona.

Claim 56 recites:

> A method comprising:
>
> powering on a monotonic counter, the monotonic counter at least partially basing a count value on a content of a volatile memory and a non-volatile memory; and
>
> updating the count value for the monotonic counter on the powering on condition by utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.

For the reasons described above with respect to claim 48, claim 56 is patentable over Incardona. because claim 57 depends from claim 56 and includes additional limitations, claim 57 is also patentable over Incardona.

Claim 58 recites:

> An apparatus comprising:
>
> a volatile counter to maintain a first value;
>
> a non-volatile counter to maintain a second value based on a content of a non-volatile memory; and
>
> control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count.

For the reasons described above with respect to claim 48, claim 58 is patentable over Incardona. Claims 59-63 depend from claim 58 and include additional limitations. Thus, claims 59-63 are also patentable over Incardona.

Claim 64 recites:

> An apparatus comprising:
>
> a volatile memory to maintain a first value for a first counter;
>
> a non-volatile memory to maintain a second value for a second counter; and
>
> circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on the first value for lesser significant bits of the count value and the second value for higher significant bits of the count value, and to update the count value by a number in response to a read of the count value for the monotonic counter.

For the reasons described above with respect to claim 48, claim 64 is patentable over Incardona. Since claims 65 and 66 depend from claim 64 and include additional limitations, claims 65 and 66 are also patentable over Incardona.

Claim 67 recites:

> An apparatus comprising:
> a volatile memory to maintain a first value for a first counter;
> a non-volatile memory to maintain a second value for a second counter; and
> circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on the first value for lesser significant bits of the count value and the second value for higher significant bits of the count value, and to update the count value by a number in response to a powering on condition for the circuitry.

For the reasons described above with respect to claim 48, claim 67 is patentable over Incardona. Because claims 68 and 69 depend from claim 67 and include additional limitations, claims 68 and 69 are also patentable over Incardona.

Claim 70 recites:

> An apparatus comprising:
> one or more registers to store a first value;
> a first adder to maintain the first value;
> a flash memory to store a portion of bits used for a monotonic count;
> one or more registers to store a second value;
> a second adder to maintain the second value based on one or more programmed locations in the flash memory; and
>
> a control engine to control the flash memory and the first and second adders, the first value used to determine lower significant bits of the monotonic count and the second value used to determine higher significant bits of the monotonic count, the lesser significant bits being volatile while higher significant bits being non-volatile.

For the reasons described above with respect to claim 48, claim 60 is patentable over Incardona. Because claims 71 and 72 depend from claim 70 and include additional limitations, claims 71 and 72 are also patentable over Incardona.

Claim 73 recites:

> A computer system comprising:
>
> (a) a monotonic counter comprising:
>
> (i) a volatile counter to maintain a first value,
>
> (ii) a non-volatile counter to maintain a second value based on a content of a non-volatile memory, and
>
> (iii) control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count; and
>
> (b) one or more processors to read the first and second values.

For the reasons described above with respect to claim 48, claim 73 is patentable over Incardona. Claim 74-76 depend from claim 73 and include additional limitations. Therefore, claims 74-76 are also patentable over Incardona.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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